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Docket No.: 200210236-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Brian M. Johnson et al.

Application No.: 10/765,581 | Confirmation No.: 1503

Filed: January 27, 2004 | Art Unit: 2113

For: SYSTEM AND METHOD USING A PROGRAMMABLE DEVICE FOR CAPTURING SIGNALS FROM A DEVICE DURING TESTING | Examiner: Y. L. Wilson

SUPPLEMENTAL APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Per a Notification of Non-Compliant Appeal Brief mailed on November 6, 2007, the applicants submit the following Supplemental Appeal Brief. The applicants note that this Supplemental Appeal Brief changes the status of claims 5 and 6 to objected to. Accordingly, claims 5 and 6 are no longer appealed.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

VII. Argument
VIII. Claims Appendix
IX. Evidence Appendix
X. Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Limited Partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 25 claims pending in application.

B. Current Status of Claims

1. Claims canceled: None

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 1-25

4. Claims allowed: None

5. Claims objected to: 3-6, which are indicated as being allowable if rewritten in independent form.

6. Claims rejected: 1,2 and 7-25

C. Claims On Appeal

The claims on appeal are claims 1, 2, and 7-25

IV. STATUS OF AMENDMENTS

A Second Office Action rejecting claims 1, 2, and 5-25 of the present application was mailed March 7, 2007. In response, Applicant filed a Notice of Appeal, which this brief supports. Additionally, Applicant filed an amendment on July 26, 2007 which amended claim 5 to remove the word "the" before the word "order" in order to resolve a lack of antecedent basis rejection raised for that claim in the Second Office Action. The Amendment to claim 5 has been entered. Accordingly, the claims on appeal are those as rejected in the Second Office Action of March 7, 2007, except for claims 5 and 6 which are now objected to. Therefore, claims 1, 2, and 7-27 are appealed herein. A complete listing of the claims is provided in the Claims Appendix hereto.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the separately argued claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. It should be noted that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

According to one claimed embodiment, such as that of independent claim 1, a system comprises a first device (e.g., DUT 102 of FIG. 1) arranged on a circuit board (e.g., circuit board 101 of FIG. 1). The system further comprises a programmable capture device (e.g., FPGA 103 of FIG. 1) arranged on said circuit board, wherein at least one input pin of said programmable capture device (e.g., pin 103E of FPGA 103 of FIG. 1) is communicatively coupled to at least one externally-accessible signal pin of said first device (e.g., pin 102E of DUT 102 of FIG. 1) such that said programmable capture device captures at least one signal from said first device during testing of said first device. *See e.g.,* paragraphs 0009 and 0018-0028 of the specification.

In certain embodiments, such as that of dependent claim 2, the first device is arranged on a first side of said circuit board, and the programmable capture device is arranged on a side of said circuit board opposite said first side, *see e.g.*, the example of FIG. 1 where DUT 102 is on one side of circuit board 101 and FPGA 103 is on an opposite side thereof, and *see* paragraph 0018 of the specification.

In certain embodiments, such as that of dependent claim 5, the programmable capture device has a density of input pins on order of signal pins of said first device, *see e.g.,* paragraph 0020 of the specification.

According to another claimed embodiment, such as that of independent claim 15, a method comprises triggering testing of a first device (e.g., DUT 102 of FIG. 1) arranged on a circuit board (e.g., circuit board 101 of FIG. 1), *see* block 801 of FIG. 8. The method further comprises capturing data from an externally-accessible signal pin of said first device (e.g., pin

102E of DUT 102 of FIG. 1) during said testing by a separate field-programmable data capture device (e.g., FPGA 103 of FIG. 1) also arranged on said circuit board, *see* block 802 of FIG. 8. *See e.g.,* paragraphs 0010 and 0041 of the specification.

According to another claimed embodiment, such as that of independent claim 21, a system comprises a first means (e.g., DUT 102 of FIG. 1) for performing an operation, wherein said first means is arranged on a circuit board (e.g., circuit board 101 of FIG. 1). The system further comprises a means (e.g., FPGA 103 of FIG. 1) external to said first means, arranged on said circuit board, for capturing signals from an externally-accessible pin of said first means (e.g., pin 102E of DUT 102 of FIG. 1) during testing of said first means, wherein the capturing means is programmable while arranged on said circuit board. *See e.g.,* paragraphs 0011 and 0018-0028 of the specification.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 2 7-9, and 15-25 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Publication Number 20030110429A1 to Bailis et al. (hereinafter "*Bailis*").

B. Claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Bailis* in view of U.S. Patent No. 5,530,706 to Josephson et al. (hereinafter "*Josephson*").

C. Claims 11-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Bailis* in view of *Josephson* and further in view of U.S. Patent No. 4,558,422 to DenBeste et al. (hereinafter "*DenBeste*").

ARGUMENT

Appellant respectfully traverses the outstanding rejections of the pending claims, and requests that the Board reverse the outstanding rejections in light of the remarks contained herein. The claims do not stand or fall together. Instead, Appellant presents separate arguments for various claims. Each of these arguments is separately argued below and presented with separate headings and sub-heading as required by 37 C.F.R. § 41.37(c)(1)(vii).

A. Rejections Under 35 U.S.C. §102(e) over *Bailis*

Claims 1, 2 7-9, and 15-25 are rejected under 35 U.S.C. §102(e) as being anticipated by *Bailis*. To anticipate a claim under 35 U.S.C. § 102, a single reference must teach every element of the claim, *see* M.P.E.P. § 2131. Appellant respectfully traverses this rejection and requests that it be overturned because *Bailis* fails to teach all elements of claims 1, 2 7-9, and 15-25, as discussed below.

Independent Claim 1 and Dependent Claims 7-9

Independent claim 1 recites:

> A system comprising:
> a first device arranged on a circuit board; and
> a programmable capture device arranged on said circuit board, wherein at least one input pin of said programmable capture device is communicatively coupled to at least one externally-accessible signal pin of said first device such that said programmable capture device captures at least one signal from said first device during testing of said first device. (Emphasis added).

Bailis fails to teach all of the above elements of claim 1. For instance, *Bailis* fails to teach a programmable capture device that is communicatively coupled to at least one externally-accessible signal pin of a first device arranged on a circuit board. Rather, *Bailis* is directed to an ASIC that includes an internal programmable device for capturing signals within the ASIC that are not accessible via an externally-accessible signal pin of the ASIC. For instance, *Bailis* explains in paragraph 0003:

> In today's test environment, application specific integrated circuits (ASICs) are extremely dense with various functions while having a limited number of I/O pins with respect to those functions. Often, there are significant, complex functions connected with only internal ASIC buses and signal paths, which are not exposed via an I/O pin. Further, due to the density and complexity of functions, it would not be practical to bring out all needed functions for observation and control, as this would result in potentially thousands of I/O pins. (Emphasis added).

Thus, *Bailis* recognizes that ASICs include many internal functional components that are not accessible via external pins of the ASIC, nor is it practical to expose all of the functional components via external pins because of the large number of I/O pins that would require. However, *Bailis* goes on to explain that a desire arises for testing such internal functional components of an ASIC that are not exposed via an external pin of the ASIC.

Paragraphs 0012 and 0013 of *Bailis* further explain:

> Historically, functional entities were embodied in multiple modules with an exposed bus and signal paths between the modules. This enables the use of logical analyzers, logic debuggers and like tools to be used to observe and control the system. With the advent of integration techniques, multiple modules and their interconnections are now placed inside a single chip, often an ASIC. Because of this integration, the use of these tools (external logical analyzers, logic debuggers and like tools) is not possible with today's ASICs, as there is no physical method available to place the tools on an internal-to-the-ASIC bus and no method to disconnect and tie up or down internal-to-the-ASIC signal paths to provide the observation and control of the functions.
>
> Accordingly, what is needed is a system and method for allowing the observation and control of an ASIC that allows for placing tools internal to the ASIC without requiring additional I/O pins. The system should be easy to implement, cost effective and easily adaptable to standard cell IC design tool. The present invention addresses such a need. (Emphasis added).

In view of the above, *Bailis* recognizes a desire for testing internal functional components of an ASIC without requiring addition of externally-accessible pins for exposing such internal functional components external to the ASIC. Thus, *Bailis* is concerned with observing internal signals of internal functional components of an ASIC that do not have externally-accessible signal pins. As such, the functional component (or "first device" in the nomenclature of claim 1) that is being tested in *Bailis* is one which does not have an externally-accessible signal pin to

which a capture device can couple for observing signals thereof during testing. Accordingly, as discussed further below, *Bailis* proposes implementing a field-programmable gate array (FPGA) within the ASIC to enable observation and control of certain internal functional components of the ASIC that do not comprise an externally-accessible signal pin.

Indeed, the entire reason for the implementation of the FPGA solution in *Bailis* is because, as discussed above, the internal functional components of the ASIC that are desired to be tested lack an externally-accessible signal pin. Thus, *Bailis* proposes implementing an FPGA "to create an internal-to-the-ASIC bridging of internal signals to observe and control of the internal signals of the ASIC." Paragraph 0015 of *Bailis*. Thus, the FPGA of *Bailis* provides a bridge to enable observation and control of signals of internal functional components of an ASIC that lack externally-accessible signal pins.

In view of the above, the FPGA (or "programmable capture device arranged on said circuit board" in the nomenclature of claim 1) of *Bailis* is not communicatively coupled to an externally-accessible signal pin of an internal functional component that is being tested (or the "first device" of claim 1) because, as discussed above, such internal functional component does not have such an externally-accessible signal pin (which is the entire reason for the inclusion of the internal FPGA of *Bailis*). *Bailis* is thus not concerned with capturing signals from an externally-accessible signal pin of a device under test, which may in some instances (as discussed in the present application) contain many (e.g., thousands) of I/O pins. Instead, the FPGA (or "programmable capture device arranged on said circuit board") of *Bailis* is coupled to internal functional components of the ASIC that lack externally-accessible signal pins.

Accordingly, in view of the above, Appellant respectfully submits that *Bailis* fails to teach all elements of claim 1, and therefore the rejection of claim 1 should be overturned.

Claims 7-9 each depend either directly or indirectly from independent claim 1, and are thus likewise believed to be allowable at least based on their dependency from claim 1 for the reasons discussed above. Accordingly, Appellant respectfully requests that the rejection of claims 7-9 also be overturned.

Dependent Claim 2

Dependent claim 2 depends from claim 1, and thus inherits all of the limitations of claim 1 in addition to its own supplied limitations. It is respectfully submitted that dependent claim 2 is allowable at least because of its dependence from claim 1 for the reasons discussed above.

Further, dependent claim 2 recites further elements not taught by *Bailis*. For instance, dependent claim 2 recites "wherein said first device is arranged on a first side of said circuit board, and wherein said programmable capture device is arranged on a side of said circuit board opposite said first side." *Bailis* fails to teach this further element of claim 2. Instead, *Bailis* teaches a programmable capture device that is arranged internal to an ASIC, and is not arranged on an opposite side of a circuit board from a first device (e.g., internal component of the ASIC) from which the programmable capture device captures signals for testing of such internal device.

Thus, for this further reason, the rejection of claim 2 is improper and should be overturned.

Independent Claim 15 and Dependent Claims 16-20

Independent claim 15 recites:

> A method comprising:
> triggering testing of a first device arranged on a circuit board; and
> capturing data from an externally-accessible signal pin of said first device during said testing by a separate field-programmable data capture device also arranged on said circuit board. (Emphasis added).

Bailis fails to teach all of the above elements of claim 15. For instance, *Bailis* fails to teach capturing data from an externally-accessible signal pin of a first device by a separate field-programmable data capture device that is arranged on a circuit board. As discussed above with claim 1, *Bailis* proposes a programmable data capture device (e.g., FPGA) that is arranged internal to an ASIC for capturing signals of internal functional components of the ASIC that lack externally-accessible signal pins. Thus, the FPGA of *Bailis* does not capture data from an externally-accessible signal pin of a device that is being tested.

Additionally, claim 15 recites that the capturing of data from an externally-accessible pin of a first device is "by a separate field-programmable data capture device". Thus, even though in *Bailis* the ASIC itself has externally-accessible signal pins to which the FPGA may be coupled, the FPGA is included internally within such ASIC in *Bailis* and is thus not "a separate field-programmable data capture device". In addition, as mentioned above, the FPGA of *Bailis* does not capture data from a device being tested via any externally-accessible signal pin of the ASIC.

Accordingly, in view of the above, Appellant respectfully submits that *Bailis* fails to teach all elements of claim 15, and therefore the rejection of claim 15 should be overturned.

Claims 16-20 each depend either directly or indirectly from independent claim 15, and are thus likewise believed to be allowable at least based on their dependency from claim 15 for the reasons discussed above. Accordingly, Appellant respectfully requests that the rejection of claims 16-20 also be overturned.

Independent Claim 21 and Dependent Claims 22-25

Independent claim 21 recites:

> A system comprising:
> a first means for performing an operation, wherein said first means is arranged on a circuit board; and
> a means external to said first means, arranged on said circuit board, for capturing signals from an externally-accessible pin of said first means during testing of said first means, wherein the capturing means is programmable while arranged on said circuit board. (Emphasis added).

Bailis fails to teach all of the above elements of claim 21. For instance, *Bailis* fails to teach a first means and a means external to a first means that are arranged on a circuit board where the means external to the first means captures signals from an externally-accessible signal pin of the first means during testing of the first means. As discussed above with claim 1, *Bailis* proposes a programmable data capture device (e.g., FPGA) that is arranged internal to an ASIC for capturing signals of internal functional components of the ASIC that lack externally-accessible signal pins. Thus, the FPGA of *Bailis* does not capture data from an externally-accessible signal pin of a device that is being tested.

Additionally, claim 21 recites that the means for capturing is a means "external to said first means" from which the signals are captured. Thus, even though in *Bailis* the ASIC itself has externally-accessible signal pins to which the FPGA may be coupled, the FPGA is included internally within such ASIC in *Bailis* and is thus not "external to said first means" having the externally-accessible pin. In addition, as mentioned above, the FPGA of *Bailis* does not capture data from a device being tested via any externally-accessible signal pin of the ASIC.

Accordingly, in view of the above, Appellant respectfully submits that *Bailis* fails to teach all elements of claim 21, and therefore the rejection of claim 21 should be overturned.

Claims 22-25 each depend either directly or indirectly from independent claim 21, and are thus likewise believed to be allowable at least based on their dependency from claim 21 for the reasons discussed above. Accordingly, Appellant respectfully requests that the rejection of claims 22-25 also be overturned.

B. Rejection Under 35 U.S.C. §103(a) over *Bailis* in view of *Josephson*

Claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Bailis* in view of *Josephson*. Dependent claim 10 depends from independent claim 1 and, thus, inherits all of the limitations of claim 1. Therefore, *Bailis* does not teach or suggest all claim limitations of claim 10 for the reasons discussed above with claim 1. The Second Office Action does not rely on *Josephson* to teach or suggest the features shown to be missing from *Bailis*, nor does *Josephson* teach or suggest those features. Therefore, the rejection of claim 10 should likewise be overturned.

C. Rejections Under 35 U.S.C. §103(a) over *Bailis* in view of *Josephson* and further in view of *DenBeste*

Claims 11-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Bailis* in view of *Josephson* and further in view of *DenBeste*. Dependent claims 11-14 each depends from independent claim 1 and, thus, each of these claims inherits all of the limitations of claim 1. Therefore, *Bailis* does not teach or suggest all claim limitations of claims 11-14 for the reasons discussed above with claim 1. The Second Office Action does not rely on *Josephson* or *DenBeste* to teach or suggest the features shown to be missing from *Bailis*, nor do they do so. Therefore, the rejection of claims 11-14 should likewise be overturned.

Conclusion

In view of the above, Appellant requests that the board overturn the outstanding rejections of claims 1, 2, and 7-25. Attached hereto are a Claims Appendix, Evidence Appendix, and Related Proceedings Appendix. As noted in the attached Evidence Appendix, no evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted. Also, as noted by the Related Proceedings Appendix, no related proceedings are referenced in II above, and thus no copies of decisions in related proceedings are provided.

In view of the above, all of the pending claims are now believed to be in condition for allowance and a notice to that effect is earnestly solicited.

Respectfully submitted,
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VIII. CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 10/765,581

1. A system comprising:

a first device arranged on a circuit board; and

a programmable capture device arranged on said circuit board, wherein at least one input pin of said programmable capture device is communicatively coupled to at least one externally-accessible signal pin of said first device such that said programmable capture device captures at least one signal from said first device during testing of said first device.

2. The system of claim 1 wherein said first device is arranged on a first side of said circuit board, and wherein said programmable capture device is arranged on a side of said circuit board opposite said first side.

3. The system of claim 2 wherein said programmable capture device comprises pins having an arrangement corresponding to an arrangement of pins of the first device.

4. The system of claim 3 wherein said first device comprises at least one-thousand signal pins.

5. The system of claim 1 wherein said programmable capture device has a density of input pins on order of signal pins of said first device.

6. The system of claim 5 wherein said first device comprises at least one-thousand signal pins.

7. The system of claim 1 wherein said first device comprises an Application-Specific Integrated Circuit (ASIC).

8. The system of claim 1 wherein said programmable capture device comprises a Field Programmable Gate Array (FPGA).

9. The system of claim 1 further comprising:

at least one output pin of said programmable capture device communicatively coupled to

an interface for a logic analyzer that is external to said circuit board, wherein said interface is arranged on said circuit board.

10. The system of claim 9 wherein said testing of said first device comprises testing said first device at its normal operating frequency.

11. The system of claim 10 wherein said logic analyzer has an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer.

12. The system of claim 11 wherein the programmable capture device parallelizes the captured signals.

13. The system of claim 10 wherein said logic analyzer has an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer.

14. The system of claim 13 wherein the programmable capture device serializes the captured signals.

15. A method comprising:

triggering testing of a first device arranged on a circuit board; and

capturing data from an externally-accessible signal pin of said first device during said testing by a separate field-programmable data capture device also arranged on said circuit board.

16. The method of claim 15 further comprising:

outputting at least a portion of the captured data from the field-programmable data capture device to a logic analyzer arranged external to said circuit board.

17. The method of claim 15 further comprising:

programming the field-programmable data capture device to capture desired data from the first device.

18. The method of claim 17 wherein said programming comprises:

programming the field-programmable data capture device while said field-programmable data capture device is arranged on said circuit board.

19. The method of claim 17 further comprising:

communicatively coupling a control system to said field-programmable data capture device arranged on said circuit board for performing the programming.

20. The method of claim 17 wherein the programming comprises selecting at least one signal pin of said first device from which data is to be captured by said field-programmable data capture device.

21. A system comprising:

a first means for performing an operation, wherein said first means is arranged on a circuit board; and

a means external to said first means, arranged on said circuit board, for capturing signals from an externally-accessible pin of said first means during testing of said first means, wherein the capturing means is programmable while arranged on said circuit board.

22. The system of claim 21 further comprising:

a means, arranged external to said circuit board, for analyzing captured signals of the first means, wherein the analyzing means is communicatively coupled to the capturing means.

23. The system of claim 21 further comprising:

means, arranged external to said circuit board, for programming the capturing means.

24. The system of claim 23 wherein the programming comprises selecting at least one signal pin of the first means from which signals are to be captured by the capturing means.

25. The system of claim 21 wherein the capturing means comprises a plurality of input pins that are each communicatively coupled to a different signal pin of the first means, and wherein the capturing means is programmable to select at least one of said input pins that is to have its received signals output at an output pin of the capturing means.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in II above, and thus no copies of decisions in related proceedings are provided.